REMARKS

Claims 1-8 are pending. Claims 1 and 5 are independent.

Claims 1-8 have been objected to for various informalities. In response, claims 1 and 5 have been amended to address these objections. Accordingly, Applicant respectfully requests removal of this objection.

Claims 3-4 and 7-8 have been rejected under 35 U.S.C 112, first paragraph, as failing to comply with the written description requirement. In particular, that "the original disclosure does not support the concept of one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters…" In response, claims 1 & 5 have been amended to remove the cited limitations. Accordingly, applicants respectfully request removal of these rejections.

Independent claims 1 and 5 have been amended recite the limitations of: "…one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster."

These amendments in claims 1 & 5 are supported by the description on page 6, lines 25-30 and figure 3: "*Accordingly, the number of pipeline registers P between clusters can be proportional to or dependent on the distance between the respective clusters. Moreover, one or more pipeline register P are arranged in the control path CC and CD. Alternatively one or more pipeline registers P are arranged in each of the control paths CC and CD, in order to pipeline the control signals to remote clusters C;*" and page 3, lines 17-20: "*According to this instruction set architecture higher clock frequencies can be achieved, since the clock period is not limited by the longest delay in control signals due to the longest distance between the instruction unit and the most remote cluster. In other words, longer delays in the control wires to distant clusters can be adopted.*"

Claims 1-3 and 5-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US5598408). Claims 4 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

Further, the Office Action indicates that "Batten does not disclose each control connection having a pipeline register, and one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so

as to pipeline said control connections to said remote cluster," now amended to "one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance...."

The Office Action indicates that Nickolls disclose the above limitations on col. 6, lines 11-14 & col. 60, lines 1-5. Applicants respectfully disagree.

As previously noted, Nickolls teaches a scalable inter-processor messaging system for parallel processor arrays wherein the message delay characteristics of the messaging system do not increase in direct proportion to or at a faster rate than the size of the messaging system, by partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message.

For further clarity, the claims have been amended to recite "A clustered Instruction Level Parallelism processor…" instead of a "Data processing system…" Accordingly, Nickolls is not analogous art but relates to parallel processing systems and more specifically to the transmission of information through so-called massively-parallel Single Instruction Multiple Data (SIMD) computing machines and not a clustered Instruction Level Parallelism processor... as claimed. Thus, it is not seen why one

skilled in the art would look to the elements of a massively-parallel Single Instruction Multiple Data (SIMD) computing machines, although similar sounding, for use in a clustered Instruction Level Parallelism processor.

Further, Applicant respectfully submits that the Office Action has used impermissible hindsight to reject claims under 35 U.S.C. § 103(a). The Federal Circuit in *In re Rouffet* stated that virtually all inventions are combinations of old elements. Therefore an Examiner may often find many elements of a claimed invention in the prior art. To prevent the use of hindsight based on the invention to defeat patentability of the invention, the Examiner is required to show a motivation to combine the references and further a motivation to modify the combination to justify a finding of obviousness. Applicant respectfully submits that the Office Action has not met this burden.

The mere fact that the prior art device could be modified so as to produce the claimed device, is not a basis for an obviousness rejection unless the prior art suggested the desirability of the modification. See, In re Gordon, 733 F.2d 900, 902 (Fed, Cir. 1984); and In re Laskowski, 871 F.2d 115, 117 (Fed. Cir. 1989). The only suggestion that can be found anywhere for making the modification appears to come from the present patent application itself.

The Office Action further indicates that "Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path." However, this is a different problem than the present invention, and it is unclear why one skilled in the art would look to the reasons there is a need to increase the bit flow rate of the path in a so-called massively-parallel Single Instruction Multiple Data (SIMD) and use them for a clustered Instruction Level Parallelism processor. One of the problems the current invention solves is that of enabling higher clock frequencies, since the clock period is not limited by the longest delay in control signals due to the longest distance between the instruction unit and the most remote cluster.

Moreover, Applicant can nothing in Batten or Nickolls, alone or in combination, that teaches the limitations of "one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, *to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster*."

Since Batten or Nickolls, alone or in combination, does not teach all of the limitations of independent claims 1 and 5, as amended, it cannot render the present invention obvious. For at least the above cited reasons, Applicant submits that Claims 1 and 5 are patentable over Batten and Nickolls.

With regard to claims 2-4 and 6-8 these claims depend from one of the independent claims discussed above, which have been shown to be allowable in view of the cited reference. Accordingly, each of claims 2-4 and 6-8 are also allowable by virtue of its dependence from an allowable base claim. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

Applicant denies any statement, position or averment stated in the Office Action that is not specifically addressed by the foregoing. Any rejection and/or points of argument not addressed are moot in view of the presented arguments and no arguments are waived and none of the statements and/or assertions made in the Office Action is conceded.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,
Dan Piotrowski
Registration No. 42,079

/Thomas J. Onka/

Date: August 8, 2011

By: Thomas J. Onka
Attorney for Applicant
Registration No. 42,053

Mail all correspondence to:
Dan Piotrowski, Registration No. 42,079
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9624
Fax: (914) 332-0615